

D. Bricio-Blázquez<sup>1</sup>, A. Kapas<sup>1,2</sup>, A. Guerrero<sup>1</sup>, J. Sánchez<sup>1</sup>, A. García<sup>1</sup>, R. Mas<sup>1</sup>, X. Borrís<sup>3</sup>, J. Bausells<sup>1</sup>, F. Perez-Murano<sup>1</sup> and J. Llobet<sup>1</sup>

<sup>1</sup>Institute of Microelectronics of Barcelona (IMB-CNM CSIC), Bellaterra, Catalonia, E-08193, Spain

<sup>2</sup>Universitat Autònoma de Barcelona (UAB), Bellaterra, Catalonia, E-08193, Spain

<sup>3</sup>Catalan Institute of Nanoscience and Nanotechnology (ICN2), CSIC and The BIST, Bellaterra, 08193, Catalonia, Spain

e-mail: David.Bricio@imb-cnm.csic.es

## Abstract

We are developing a high throughput fabrication process of single-electron devices (SED). The SED is based on silicon nanowire (SiNW) in which a quantum dot (QD) will be generated.

The main features are:

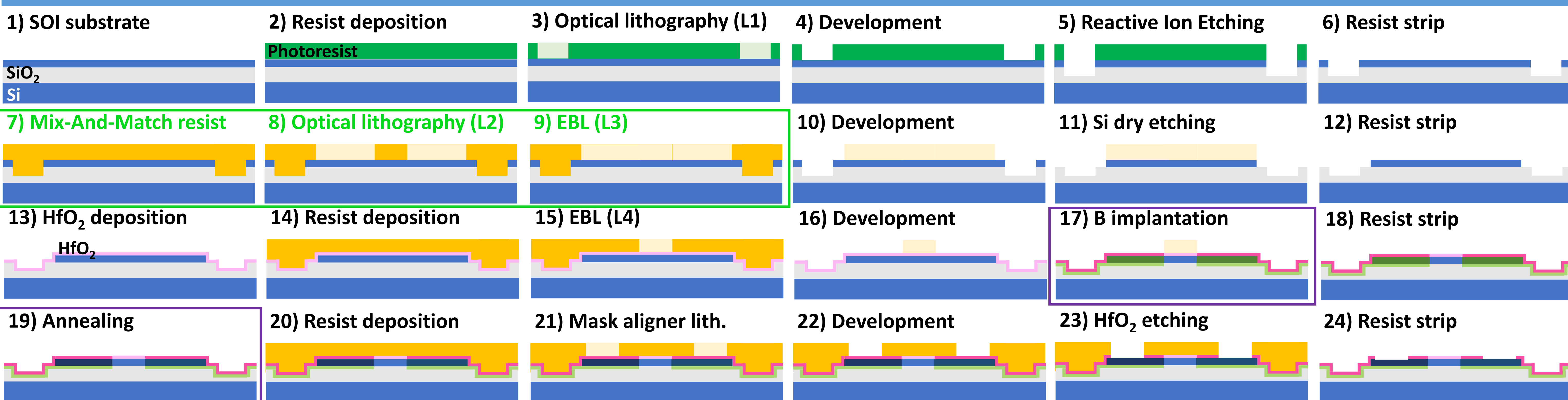
- High accuracy and dimensional control
- Mix-and-match approach based on optical and electron beam lithography (EBL) with 5 lithographic levels.
- Placement of a QD in a SiNW by means of ion implantation.

**Keywords:** SED, Quantum Dot, Nanowire, Mix-And-Match approach

## Objectives

- Produce a reliable SiNW platform to experiment novel nanofabrication process of SED.
- Fabrication at wafer scale.
- Placement of the QD in the middle of the SiNW.
- Ultimately achieve deterministic single doping.

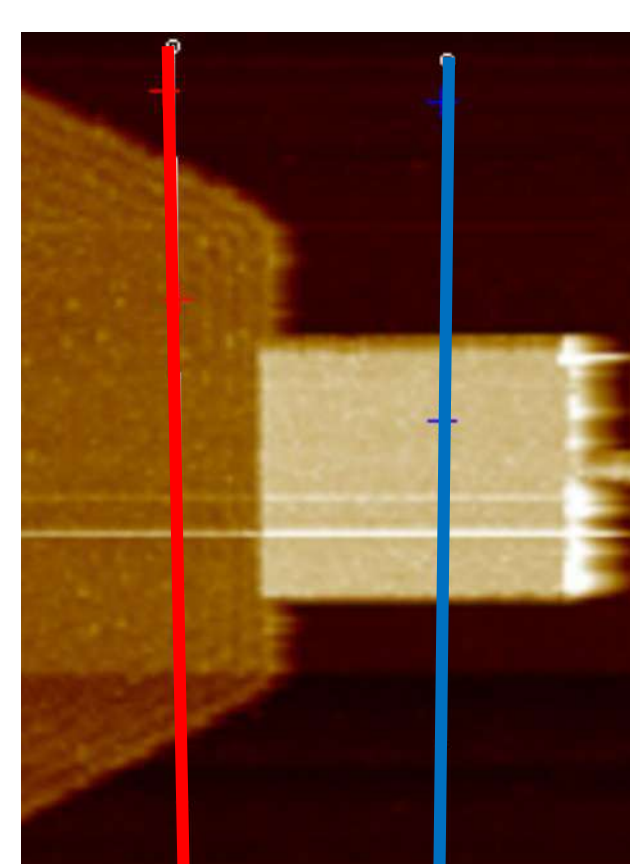
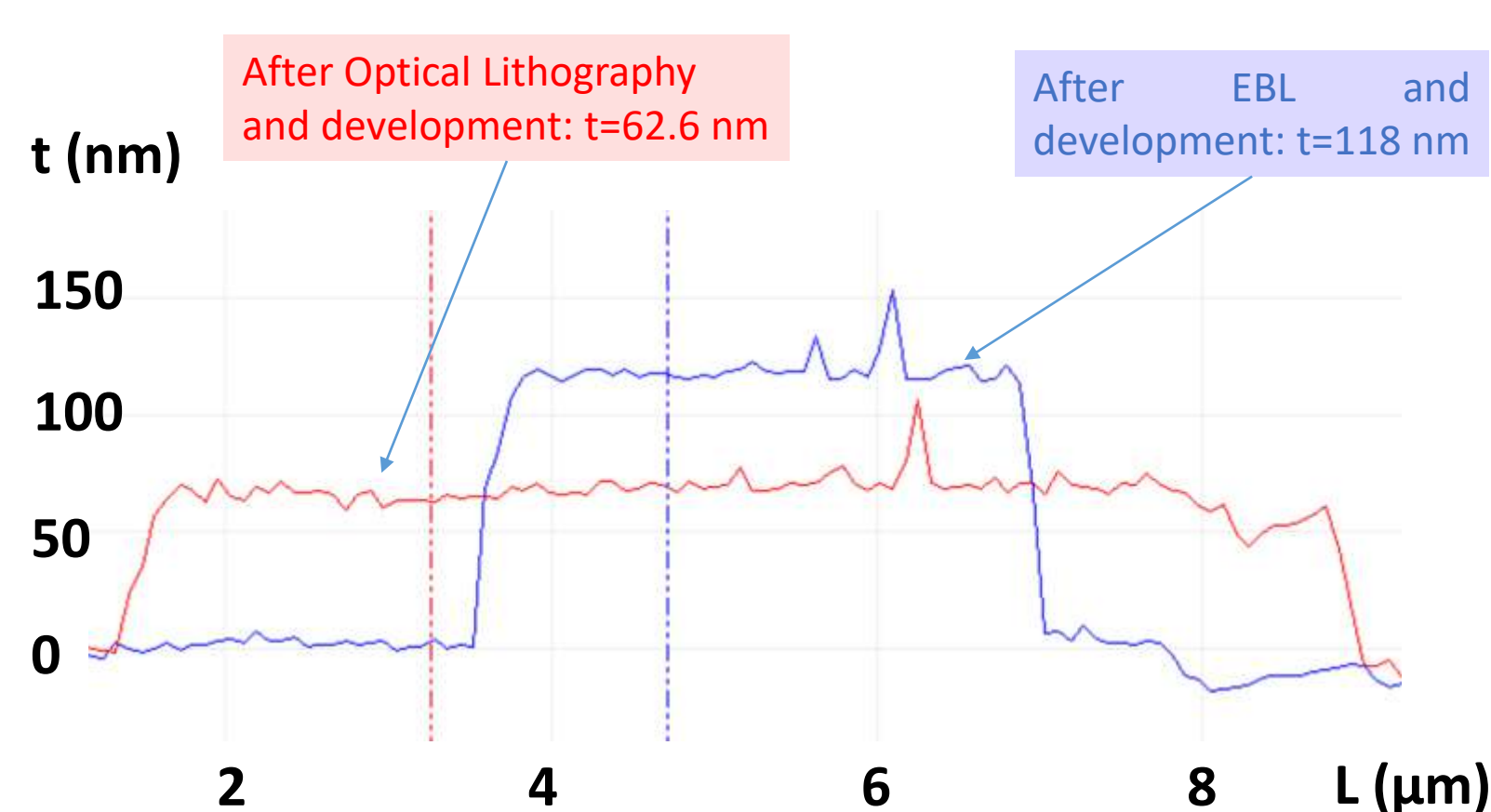
## Fabrication process



## Results

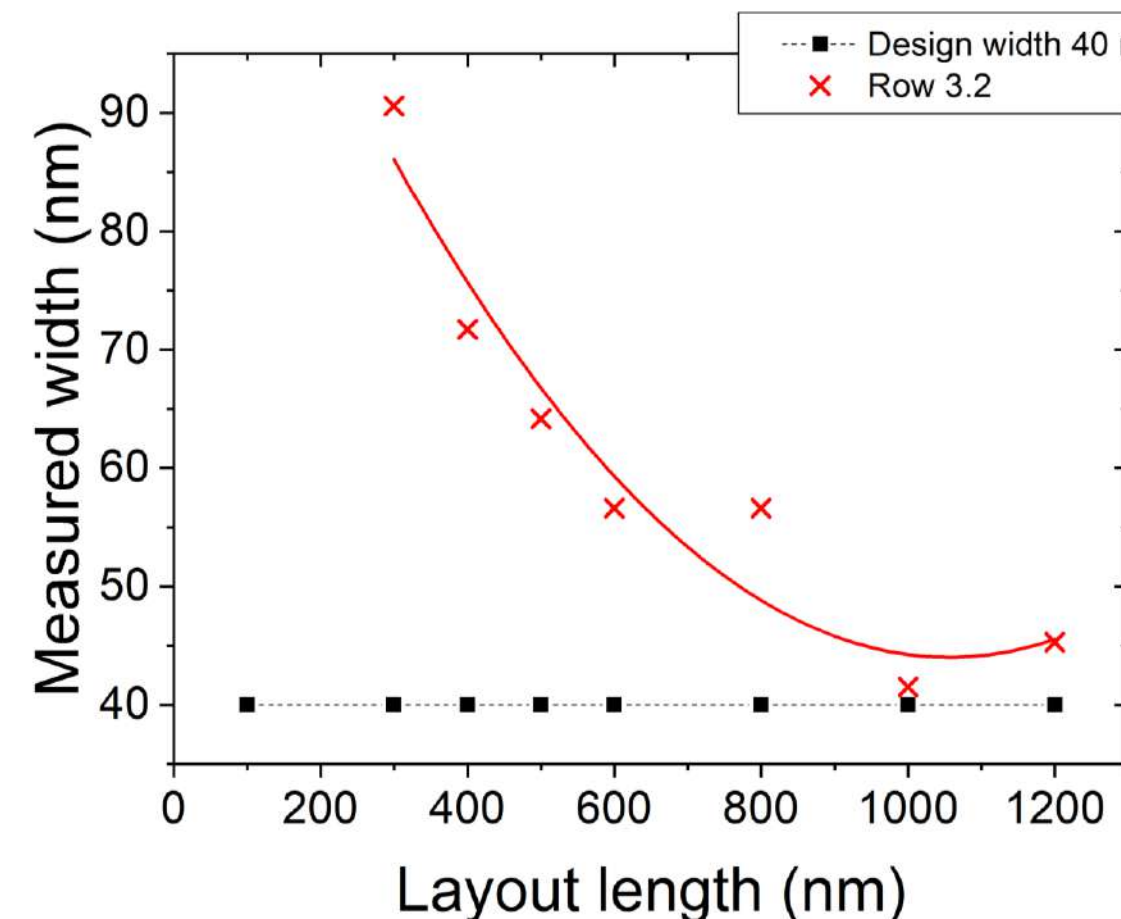
### Mix-And-Match

Height of the resist after lithography

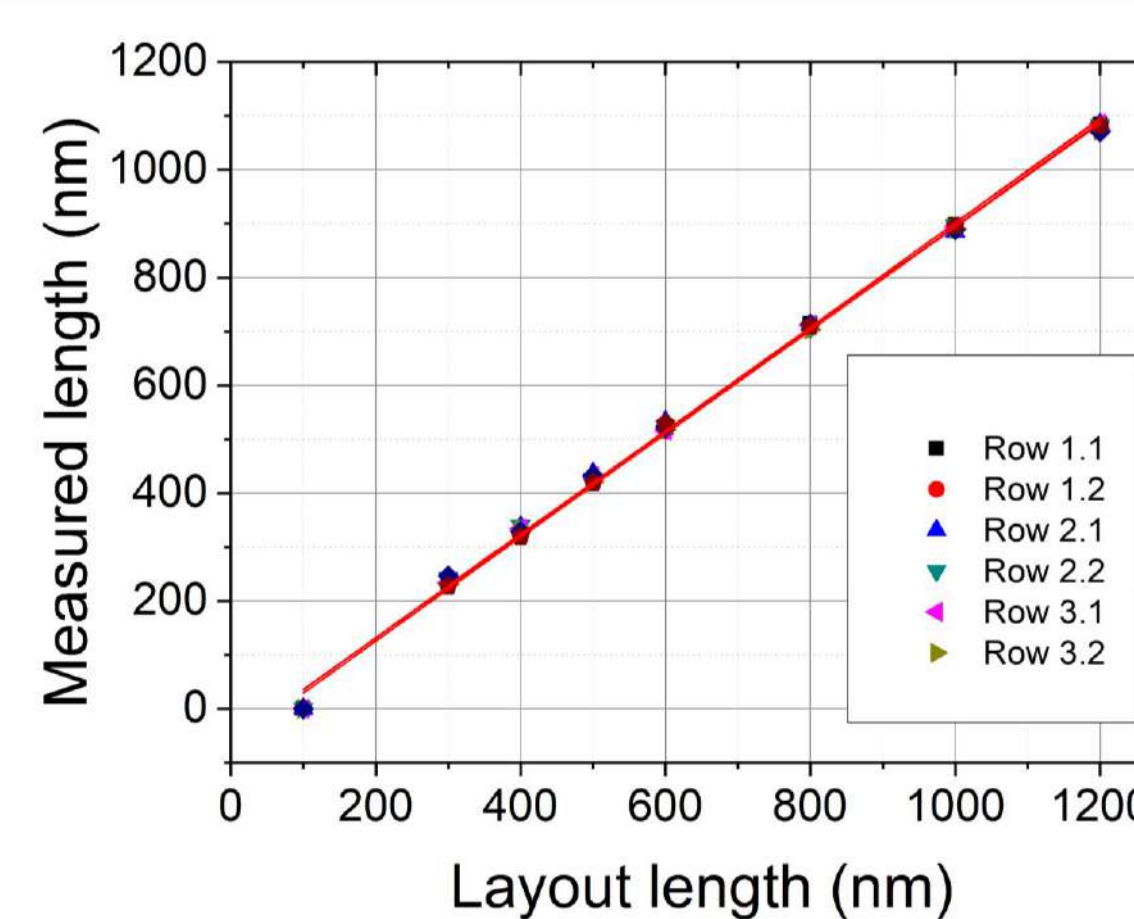


### Dimensional characterization

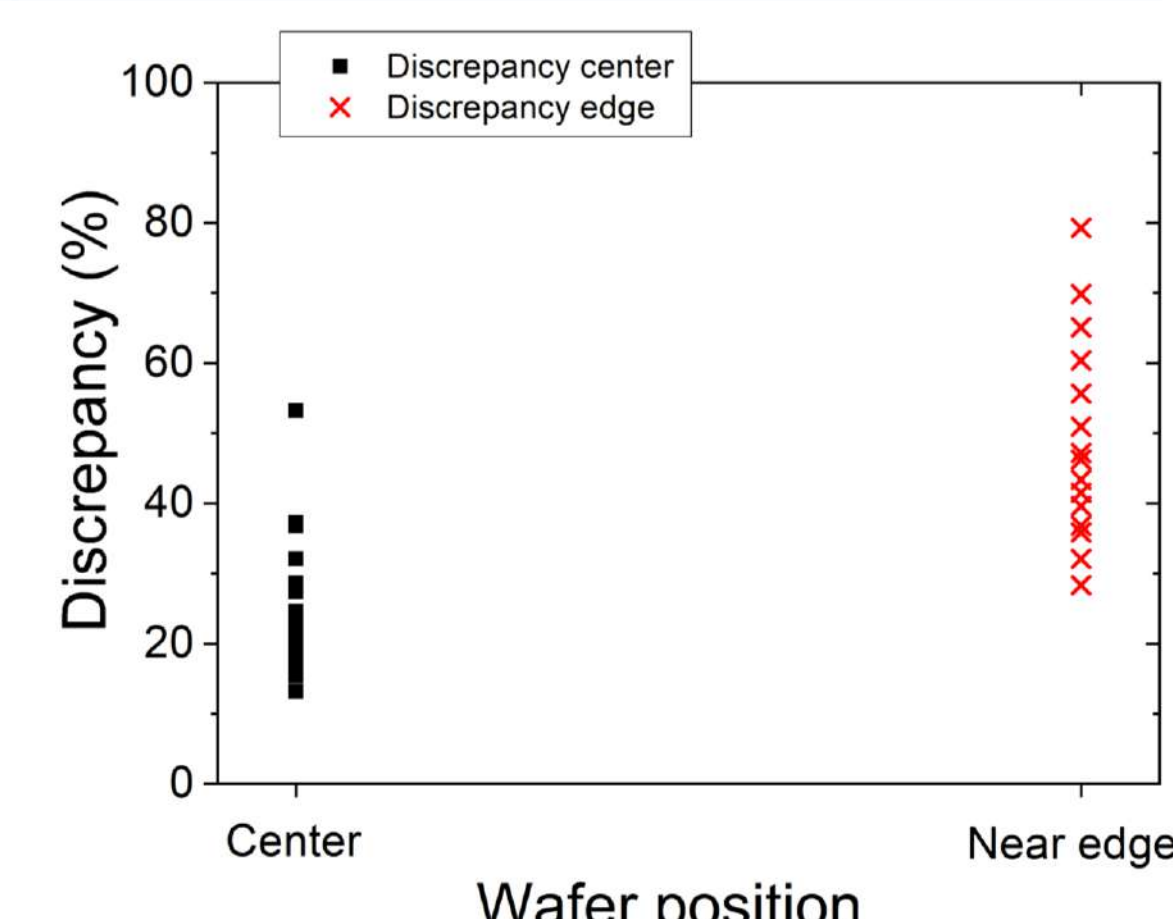
Proximity effect due to the EBL exposure



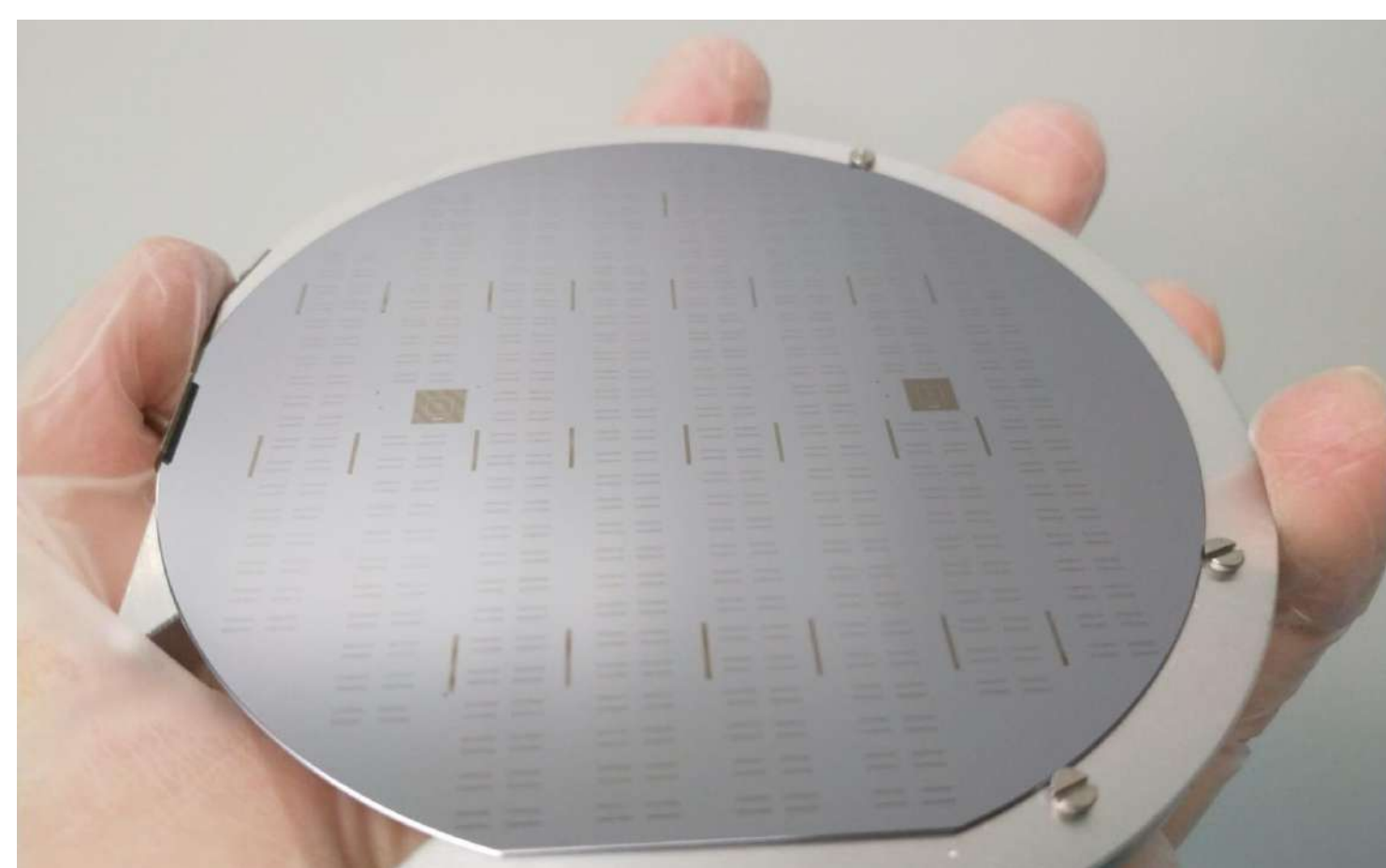
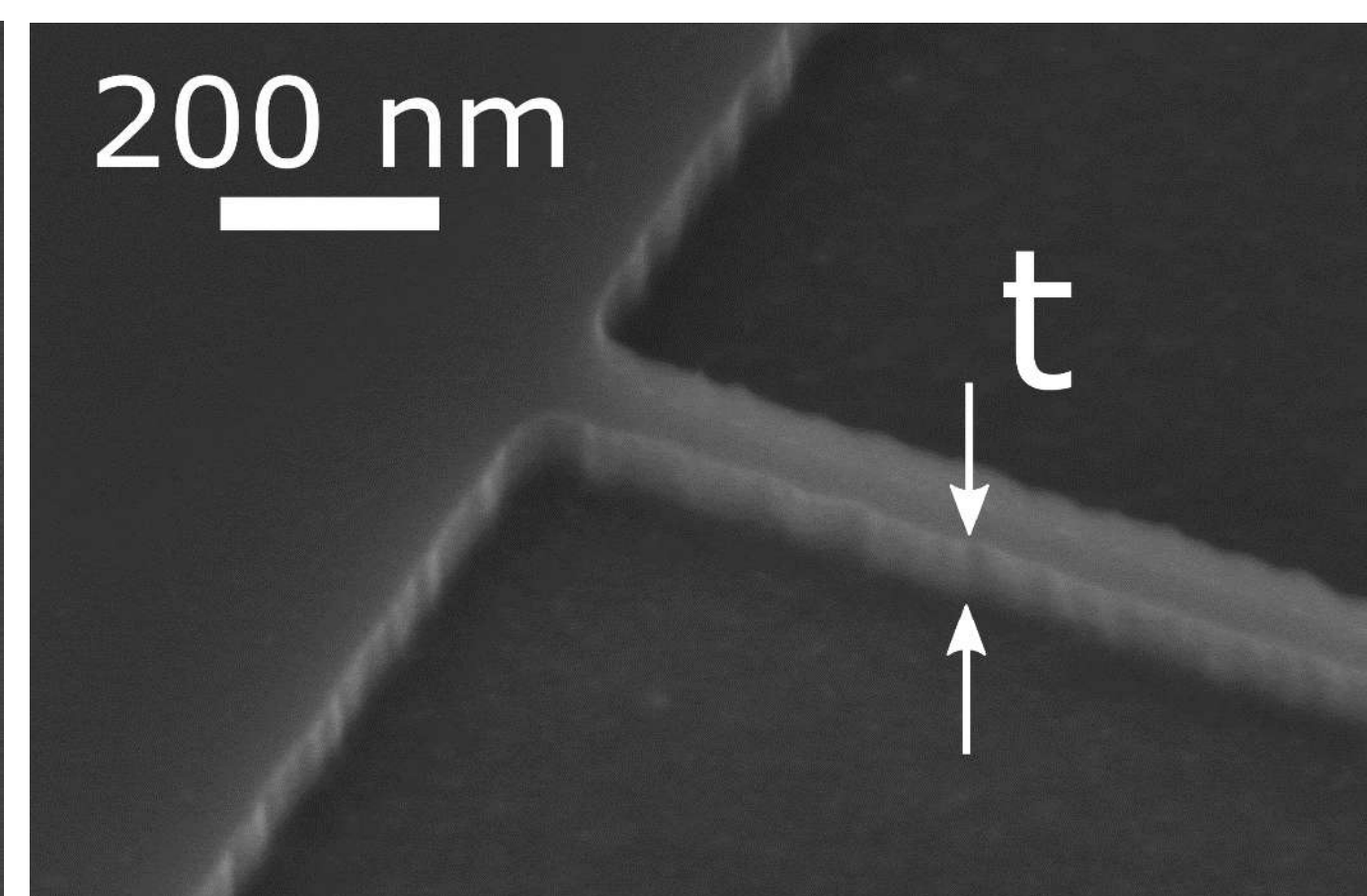
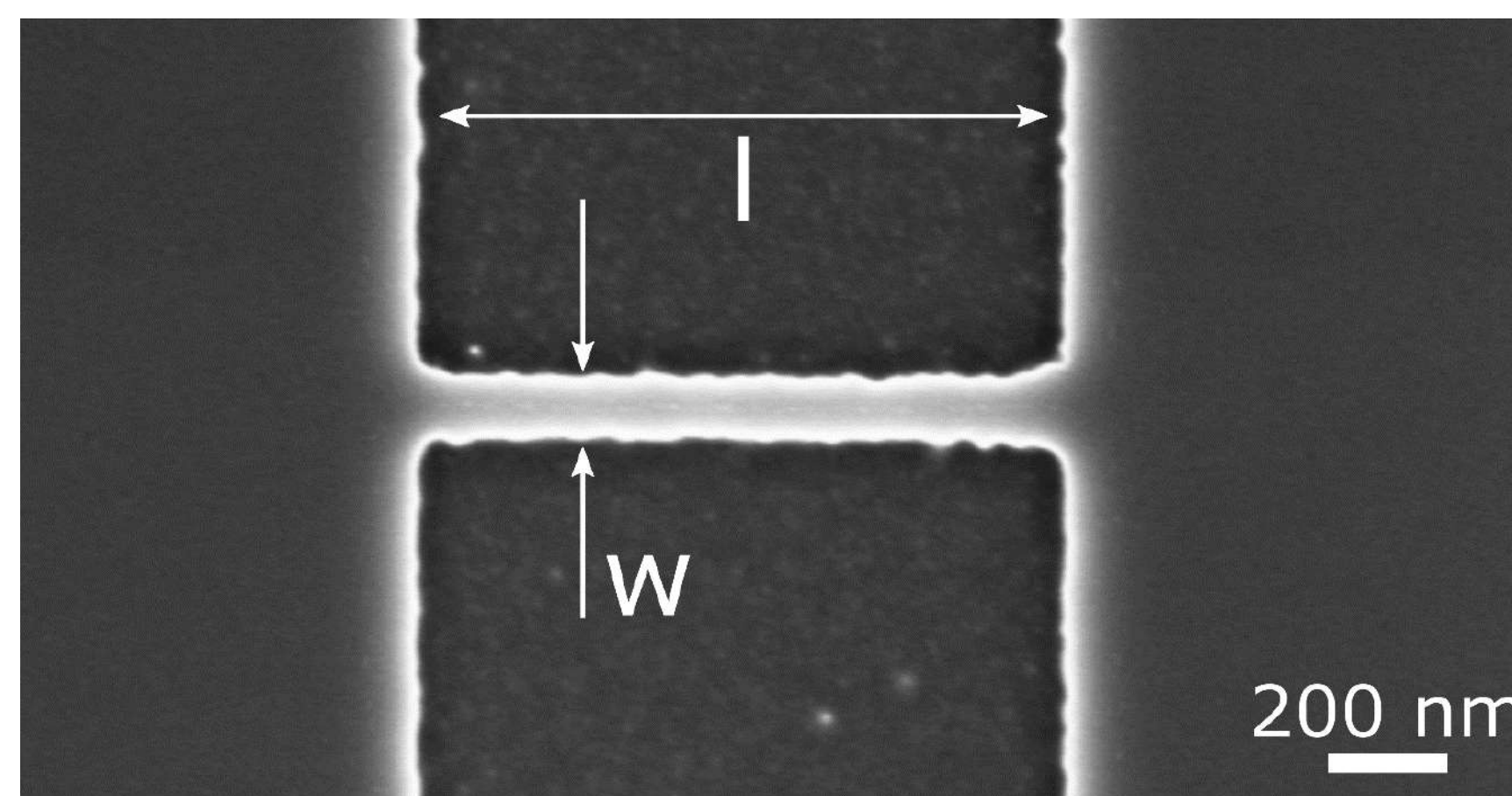
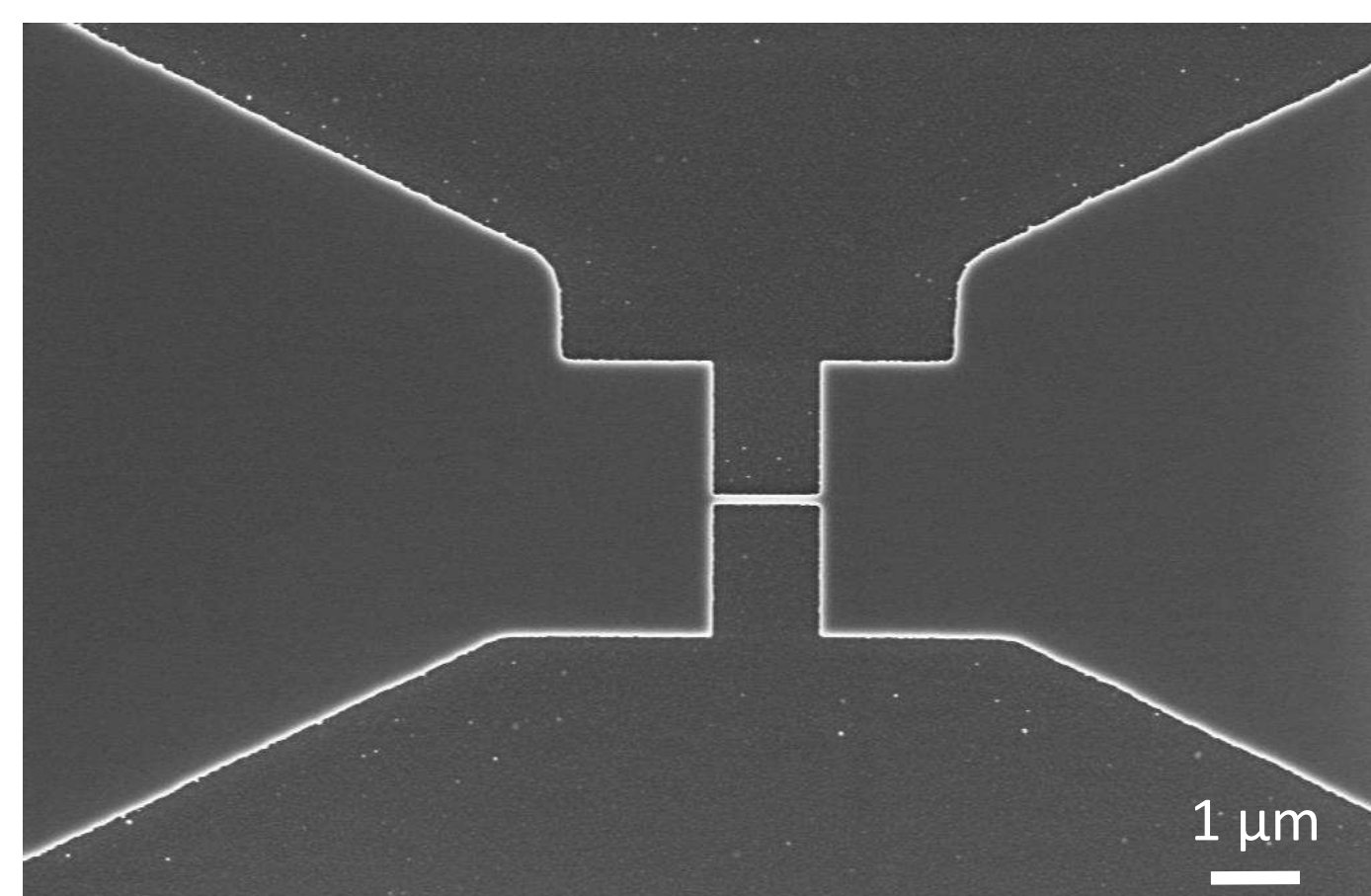
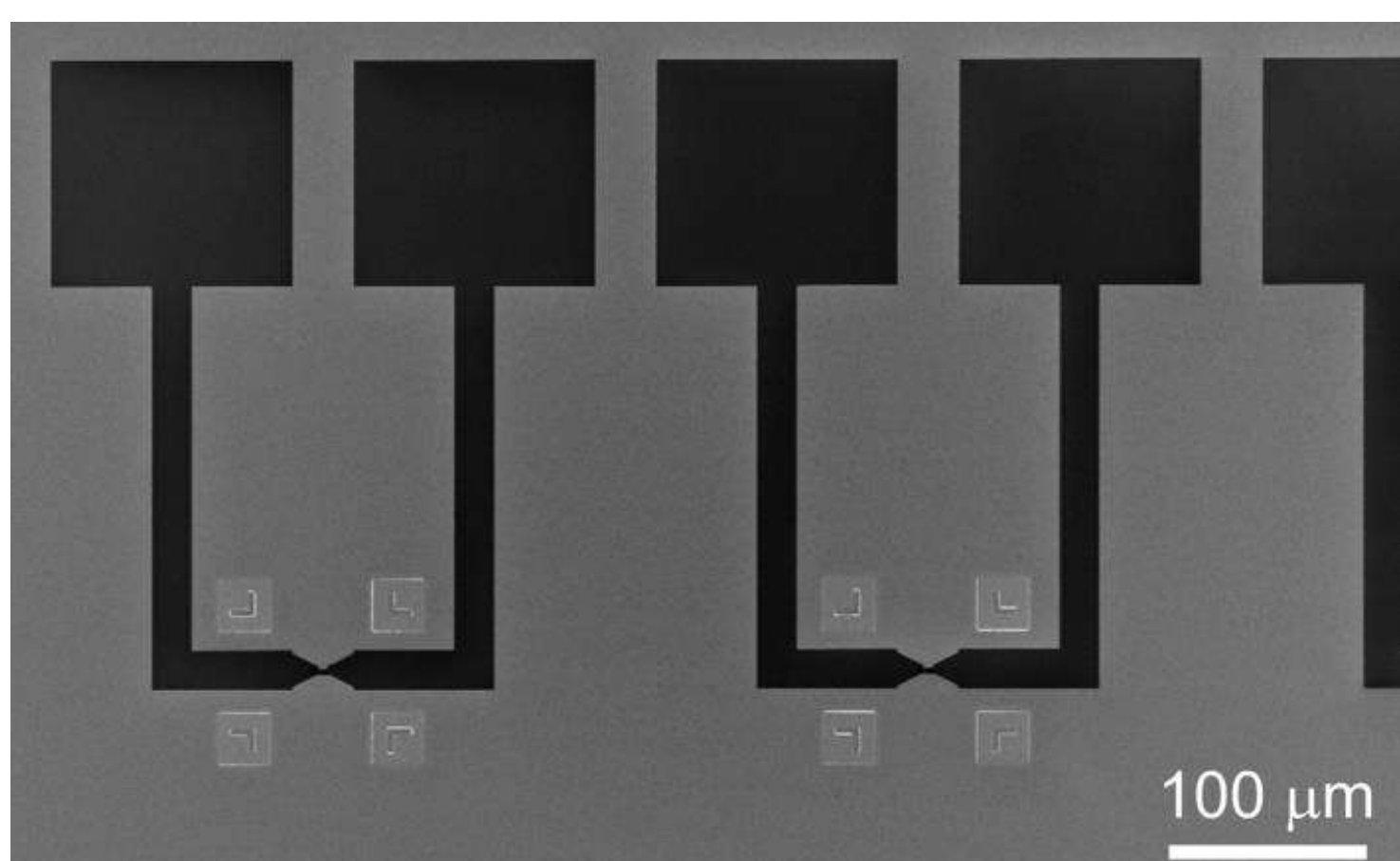
Length of the SiNWs



Uniformity analysis



## SEM characterization



## Conclusions

- Mix-and-match resist has been tuned properly.
- The alignment marks allow an appropriate alignment among the lithographic levels.
- The correlation between the layout width and the real one of the SiNWs improves as the length increases (Proximity effect is reduced).
- High throughput fabrication at wafer level has been demonstrated, getting more than 5000 individually connected SiNWs, with higher dimensional accuracy at the center of the wafer compared with the edge.

## Future work

- Continuing the process at full wafer.
- Tuning the process to reach higher agreement between the layout dimensions and the real dimensions of the nanowires.
- To improve the smoothness of nanowires.
- Continue the development of a method to place a QD in the middle of the SNW in a deterministic manner.

## Acknowledgements

Special thanks to our IMB-CNM CR engineers colleagues and the funding agencies:

NEP (Horizon 2020) – Nanoscience Foundries and Fine Analysis; STARSED Project (national funding); SiM-SeT Project (MSCA)