High throughput fabrication of Single Electron Devices based on Silicon Nanowires with embedded Quantum Dot

D. Bricio-Blázquez1, A. Kapas1,2, A. Guerrero1, J. Sánchez1, A. García1, R. Mas1, X. Borrís3, J. Bausells1, F. Perez-Murano1 and J. Llobet1
1Institute of Microelectronics of Barcelona (IMB-CNMLCIC), Bellaterra, Catalonia, E-08193, Spain
2Universitat Autònoma de Barcelona (UAB), Bellaterra, Catalonia, E-08193, Spain
3Catalan Institute of Nanoscience and Nanotechnology (ICN2), CSIC and The BIST, Bellaterra, 08193, Catalonia, Spain
e-mail: David.Bricio@imb-cnm.csic.es

Abstract

We are developing a high throughput fabrication process of single-electron devices (SED). The SED is based on silicon nanowire (SiNW) in which a quantum dot (QD) will be generated. The main features are:

- High accuracy and dimensional control
- Mix-and-match approach based on optical an electron beam lithography (EBL) with 5 lithographic levels.
- Placement of a QD in a SiNW by means of ion implantation.

Keywords: SED, Quantum Dot, Nanowire, Mix-And-Match approach

Objectives

- Produce a reliable SiNW platform to experiment novel nanofabrication process of SED.
- Fabrication at wafer scale.
- Placemnt of the QD in the middle of the SiNW.
- Ultimately achieve deterministic single doping.

Fabrication process

1) SOI substrate
2) Resist deposition
3) Optical lithography (L1)
4) Development
5) Reactive Ion Etching
6) Resist strip
7) Mix-And-Match resist
8) Optical lithography (L2)
9) EBL (L3)
10) Development
11) Si dry etching
12) Resist strip
13) HfO deposition
14) Resist deposition
15) EBL (L4)
16) Development
17) B implantation
18) Resist strip
19) Annealing
20) Resist deposition
21) Mask aligner lith.
22) Development
23) HfO etching
24) Resist strip

Results

Mix-And-Match

<table>
<thead>
<tr>
<th>Height of the resist after Lithography</th>
<th>Proximity effect due to the EBL exposure</th>
<th>Dimensional characterization</th>
</tr>
</thead>
<tbody>
<tr>
<td>t (nm)</td>
<td>t = 62.6 nm</td>
<td>t = 62.6 nm</td>
</tr>
</tbody>
</table>

Conclusions

- Mix-and-match resist has been tuned properly.
- The alignment marks allow an appropriate alignment among the lithographic levels.
- The correlation between the layout width and the real one of the SiNWs improves as the length increases (Proximity effect is reduced).
- High throughput fabrication at wafer level has been demonstrated, getting more than 5000 individually connected SiNWs, with higher dimensional accuracy at the center of the wafer compared with the edge.

Future work

- Continuing the process at full wafer.
- Tuning the process to reach higher agreement between the layout dimensions and the real dimensions of the nanowires.
- To improve the smoothness of nanowires.
- Continue the development of a method to place a QD in the middle of the SWN in a deterministic manner.

Acknowledgements

Special thanks to our IMB-CNM CR engineers colleagues and the funding agencies:
NEP (Horizon 2020) – Nanoscience Foundries and Fine Analysis;
STARTED Project (national funding); SiiM-SET Project (MSCA)